resistor R5. Current generator I_+ couples to resistor R6, and current generator I_2 coupled to the emitters of transistor M5 and transistor M6.

In one embodiment, the output duty cycle is adjusted by altering current generator I_+ or current generator L. In one embodiment, either the current from current generator I_+ or the current from current generator L is 0. The voltage where the collector of transistor M3 couples to transistor M1 is C-. Similarly, the voltage where the collector of transistor M4 couples to transistor M2 is C+.

Figure 10 illustrates signals in a duty cycle distorter in accordance with one embodiment of the present invention. Signal IN+ and signal IN- form a symmetric input signal to the duty cycle distorter. The IN+ signal crosses the IN- signal at crossing over point P1. However, signals IN+ and IN- still have the same high and low values.

The current from current generator I_+ is greater than the current from current generator L. As a result, the mean voltage of C+ falls below the mean voltage of C-. The low values for C+ are lower than the low values for C-, and the high values for C+ are lower than the high values of C-. As a result, signal C+ crosses the C- signal at crossing over point P2. Crossing over point P2 occurs later that crossing over point P1.

Signals OUT+ and OUT- are the output of the limiting amplifier of the duty cycle distorter. The positive pulse width of OUT+ is decreased and the positive pulse width of OUT- is increased. OUT+ crosses OUT- at crossing over point P3. A delay in the limiting amplifier causes crossing over point P3 to occur later than crossing over point P2. Increasing I_2 reduces the delay of the limiting amplifier. Similarly, increasing I_+ causes crossing over point P2 to occur later and results in a shorter positive pulse width for both C+ and OUT+.

The end line 1050 indicates that the signals of IN+, C+ and OUT+ all terminate at the same time. The end line does not move as a result of altering I_2 or I_+.

Figure 11 illustrates signals of a duty cycle distorter in accordance with one embodiment of the present invention. The signals used for IN+ and IN- are identical to the signals for IN+ and IN- in Figure 10. However, the current from current generator I_+ is less than the current from current generator I. As a result, the mean voltage of C+ rises above the mean voltage of C-. The low values for C+ are higher than the low values for C-, and the high values for C+ are higher than the high values of C-. Signals OUT+ and OUT- are the output of the limiting amplifier of the duty cycle distorter. The positive pulse width of OUT+ is increased and the positive pulse width of OUT- is decreased.

Series of Duty Cycle Distorters

In one embodiment, a series of duty cycle distorters, DCDs, is used to increase the pulse rise time. In one embodiment, the pulse width is not increased using DCDs. In other embodiments, the pulse width is increased using one or more DCDs. Regardless of whether the initial pulse width if increased, the pulse width is decreased by a series of DCDs. The result of each successive decreasing by a decreasing DCD is summed with the increased pulse width from the increasing DCD. The sum is the output signal of the series of DCDs. The output signal has an increased pulse rise time.

Figure 12 illustrates a series of duty cycle distorters configured to increase pulse rise time in accordance with one embodiment of the present invention. A signal 1200 is the input to DCD 1205. The output of DCD 1205 is the input for DCD 1210. Both DCD 1205 and DCD 1210 are increasing pulse width (IPW) DCDs. Thus, the original input signal has a longer pulse width due after being output from DCD 1210.

The output from DCD 1210 is an input to the summation unit 1215 as OUT1. The output from DCD 1210 is also the input to DCD 1225. Similarly, the output from DCD 1225 is an input to the summation unit as OUT2. The output from DCD 1225 is also the input to DCD 1235. Likewise, the output from DCD 1235 is an input to the summation unit as OUT3. The output from DCD 1235 is also the input to DCD 1245.

Finally, the output from DCD 1245 is an input to the summation unit as OUT4. The output from DCD 1245 is also the input to DCD 1255. Also, the output from DCD 1255 is an input to the summation unit as OUT5. DCD 1225, DCD 1235, DCD 1245 and DCD 1255 are decreasing pulse width (DPW) DCDs. Thus, the pulse width of the signal is gradually decreased as it passes through successive DWP DCDs.

The termination time of the pulse is the same in the output signals of DCD 1210, DCD 1225, DCD 1235, DCD 1245 and DCD 1255. Thus, the fall time of the sum of the signals 1265 is identical to the fall times of OUT1, OUT2, OUT3, OUT4 and OUT5. However, the pulse width gets progressively shorter as the signal passes through the series of DCDs. as a result, the initiation and completion of the rise of the signal occurs later and later with successive DCDs in the series. Thus, the sum of the signals has a rise time that is longer than the fall time. The rise time of the signal from the summation unit begins when the rise in OUT1 begins and ends when the rise in OUT5 ends.

Figure 13 illustrates the input and output signals for a summation unit in a series of duty cycle distorters in accordance with one embodiment of the present invention. The rise of a pulse in signal OUT1 begins at point P1. The rise ends at point P2. The fall of the pulse begins at point P3 and ends at point P4. Similarly, the rise of a pulse in signal OUT2 begins